ABSTRACT OF THE DISCLOSURE

A method of forming a gate in a semiconductor device includes forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device, depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially, patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer using the mask pattern as an etch barrier, forming spacers at both sidewalls of the dummy gate polysilicon layer, depositing an insulating interlayer on the resultant structure after forming the spacers, exposing a surface of the dummy gate polysilicon layer by carrying out an oxide layer CMP process having a high selection ratio against the dummy gate polysilicon layer, forming a damascene structure by removing the dummy gate polysilicon layer and the dummy gate insulating layer using the insulating interlayer as another etch barrier, depositing a gate insulating layer and a gate metal layer on the entire surface of the semiconductor substrate having the damascene structure, and exposing a surface of the insulating interlayer by carrying out a metal CMP process having a high selection ratio against the insulating interlayer.